PCN Number: 2017		7121	L4002	1	PCN Date: Dec 18, 2017		Dec 18, 2017		
				d JCAP as additiona e CMOS9T process	l Fab, Bur	np an	d As	sem	bly/Test site options
Customer Contact:		PCN	<u>Manager</u>	Dept: Quality Service		Quality Services			
Proposed 1 st Ship Date:		Mar	- 18, 2018			Date provided at sample request.			
Change Type:									
Assembly Site			Assembly Process			Assembly Materials		sembly Materials	
Design			Electrical Specification				Mechanical Specification		
Test Site			Packing/Shipping/Labeling				Test Process		
🛛 🛛 Wafer Bump Site			Wafer Bump Material				Wafer Bump Process		
🛛 🛛 Wafer Fab Site 🔹 🗍 Wafer Fab Ma		Wafer Fab Materia	als 📃 Wafer Fab Process		fer Fab Process				
				Part number change					
PCN Details									

Description of Change:

Texas Instruments is pleased to announce the addition of Aizu and JCAP as additional Fab, Bump and Assembly/Test site options for the selected devices listed in the "Product Affected" section.

Group 1 Fab Site:

C	urrent Fab Site	e	Additional Fab Site			
Current Fab Site	Process	Wafer Diameter	New Fab Site	Process	Wafer Diameter	
MAINEFAB	CMOS9T	200mm	AIZU	CMOS9T	200mm	

Group 2 Fab & Assembly/Test Site:

C	urrent Fab Site	9	Additional Fab Site			
Current Fab	Process	Wafer	New Fab	Process	Wafer	
Site		Diameter	Site		Diameter	
MAINEFAB	CMOS9T	200mm	AIZU	CMOS9T	200mm	
Current Bump/Assembly/Test Site			Additional	Bump/Assemb	ly/Test Site	
TIEM	Assembly Site	e Origin (22L)	JCAP	Assembly Sit	e Origin (22L)	
	ASO: CU6			ASO	: JCP	

Aizu and JCAP are already established Fab and Assembly/Test sites for select output voltage options of the LP5907 family of devices as was communicated in PCN 20131122000 on March 2, 2014. This PCN is to introduce additional output voltage options.

Test coverage, insertions, conditions will remain consistent with current testing and verified with test MQ. Qual details are provided in the Qual Data Section.

Reason for Change:

Continuity of supply.

Anticipated impact on Form, Fit, Function, Quality or Reliability (positive / negative):

None

Anticipated impact on Material Declaration

		-	
\boxtimes	No Impact to		Material Declarations or Product Content reports are driven from
	the Material		production data and will be available following the production
	Declaration		release. Upon production release the revised reports can be
			obtained from the <u>TI ECO website</u> .

Changes to product identification resulting from this PCN:

Current Chip Site	Chip Site Origin Code (20L)	Chip Site Country Code (21L)	Chip Site City
MAINEFAB	CUA	USA	South Portland
AIZU	CU2	JPN	Aizuwakamatsu-shi

Assembly Site		
TIEM-AT	Assembly Site Origin (22L)	ASO: CU6
JCAP-AT	Assembly Site Origin (22L)	ASO: JCP

Sample product shipping label (not actual product label)

TEXAS INSTRUMENTS MADE IN: Malaysia 20: MSL 2 /260C/1 YEAR SEAL DT 03/29/04 OPT: ITEM: BL: 5A (L)T0:1750 (1P) SN74LS07NSR (Q) 2000 (D) 0336 (31T)LOT: 3959047MLA (4W) TKY (1T) 7523483S12 (P) 120L CS0: SHE (21L) CC0:USA (21L) CC0:USA (21L) CC0:USA (21L) CC0:USA (21L) CC0:USA							
Product Affected Grou	Product Affected Group 1 (Adding Aizu Fab Site):						
LP5907UVX-1.2/NOPB	LP5907UVX-3.0/NOPB	LP5907UVX-3.1/NOPB	LP5907UVX-4.5/NOPB				
LP5907UVX-2.8/NOPB							
Product Affected Grou	p 2 (Adding Aizu Fab a	and JCAP Bump, A/T S	ite):				
LP5907UVE-1.2/NOPB	LP5907UVE-3.0/NOPB	LP5907UVE-4.5/NOPB	LP5907UVX-3.2/NOPB				
LP5907UVE-1.8/NOPB	LP5907UVE-3.1/NOPB	LP5907UVX1.875-S	LP5907UVX-3.3/NOPB				
LP5907UVE-2.7/NOPB	LP5907UVE-3.2/NOPB	LP5907UVX-2.7/NOPB	LP5907UVX37/NOPB				
LP5907UVE-2.8/NOPB	LP5907UVE-3.3/NOPB						

Qualification Report

CMOS9T 5V Process Transfer Maine to Aizu LP5907UVX-3.3 Approved: June 27, 2013

Product Attributes

Attributes			Qual Device: LP5907UVX-3.3			
Assembly Site			TIEM-MALACCA			
Package Family			YI	<e contraction="" of="" second="" second<="" td="" the=""><td></td></e>		
Flammability Rating			UL 94	1 V-0		
Wafer Fab Supplier			AIZ	20		
Wafer Process			СМО	S9T		
Moisture Sensitivity Level		LEVEL1-260C				
			Qual De	evice: LP5907UVX-	3.3	
Test Type	Conditions/D	uration	# Lots	SS/Lot	Fails	
**High Temp. Storage Bake	150C (1000 Hrs)		2	77	0	
**T/C -65C/150C	-65C/+150C (500 Cyc)	-65C/+150C (500 Cyc)		77	0	
**Unbiased HAST	130C/85%RH (96 Hrs)	130C/85%RH (96 Hrs)		77	0	
Biased Temp. Humidity	85C/85%RH (1000 Hrs)		3	77	0	
Early Life Failure Rate.	125C (48 hrs)		3	305	0	
ESD CDM	+/- 250V		3	3	0	
ESD HBM	+/- 1500V	+/- 1500V		3	0	
High Temp Operating Life	125C (1000 Hrs)	125C (1000 Hrs)		77	0	
Latchup @ 25C ,85 and 125C	(per JESD78)		3	6	0	
**Units undergo pre-conditioning before str	ess					

*Units undergo pre-conditioning before stress The following are equivalent HTOL options based on an activation energy of 0.7eV : 125C/1khrs, 140C/480hrs, 150C/300hrs, and 155C/240hrs

The following are equivalent HTSL options based on an activation energy of 0.7eV : 150C/1khrs, and 170C/420hrs The following are equivalent Temp Cycle options per JESD47 : -55C/125C/700cyc and -65C/150C/500cyc

Qualification Report

CMOS9T LP5907UVX2.85 Transfer to Aizu/JCAP

Approved: August 23, 2013

Product Attributes

Attributes			Qual Device: LP5907UVX2.85				
Assembly Site			JCAP				
Package Family				YKE			
Flammability Rating				UL 94 V-0			
Wafer Fab Supplier				AIZU			
Wafer Process				CMOS9T			
Moisture Sensitivity Level	LEVEL1-260C						
		Qual Device: LP5907UVX2.85					
Test Type	Conditions/Duration		# Lots	SS/Lot	Fails		
**T/C -65C/150C	-65C/+150C (500 Cyc)		3	77	0		
**BIASED HAST	130C/85%RH (96 Hrs)		3	77	0		
**Units undergo pre-condition - The following are equivalent	ing before stress Temp Cycle options per JESD47 : -55C/125C/700	cyc and -65C/15	50C/500cyc	1	1		

ng re equ np Cycle opti ns p су For questions regarding this notice, e-mails can be sent to the regional contacts shown below, or you can contact your local Field Sales Representative.

Location	E-Mail
USA	PCNAmericasContact@list.ti.com
Europe	PCNEuropeContact@list.ti.com
Asia Pacific	PCNAsiaContact@list.ti.com
Japan	PCNJapanContact@list.ti.com